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| EXAMINER | |
|---|---|
| SIDDIQUI, SAQIB JAVAID | |
| **ART UNIT** | **PAPER NUMBER** |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/812,580 | PORAT ET AL. | |
| | Examiner | Art Unit | |
| | Saqib J. Siddiqui | 2117 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *5-9* is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

Applicant's response was received and entered March 20, 2007.

- Claims 1-9 are pending.
- Claims 2-4 are amended.
- Claims 5-9 are allowed.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-2 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1 teaches "a logic for determining mismatches between the data and the interspersed pattern of special characters in the converted low byte parallel link and the converted high byte parallel link." It is not clear from this limitation between what signals the mismatch is being determined, since both signals include special characters and data. Applicant has claimed the same limitation in claim 3, which does not raise any 112 issues.

As per claim 2:

This claim is rejected by virtue of its dependency.

### *Response to Amendment*

Applicant's arguments and amendments with respect to claims 1-9 filed on March 20, 2007 have been considered but they are moot under new grounds of rejection.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horowitz et al. US Pat no. 7,142,612 B2 and further in view of Susnow et al. US Pat no. 6,747,997 B1.

As per claim 1:

Horowitz substantially teaches a system comprising: a transmitter board for transmitting a copy of signals produced in such system (Figure 1B), the copy of such signals comprises serial data in a low byte serial link (Figure 1B, "IN1") and in a high byte serial link (Figure 1B, "IN2"), the signals include special characters interspersed in

a pattern with the data in the low and high byte serial links (column 6, lines 40-65); a system analyzer board comprising (Figure 1B # 150): a serializer-deserializer for receiving the transmitted serial data when the analyzer board is plugged into the transmitter board (Figure 1B # 156 & 158), and for converting the received data and the special characters interspersed in both the low and high byte serial links into corresponding data and the interspersed special characters in low byte and high byte parallel links (Figure 1B, "OUT1-4").

Horowitz does not explicitly teach logic to detect alignment of the output signals and resetting the SERDES upon detection of mismatches.

However, Susnow in an analogous art teaches logic to detect the misalignment in signals (Figure 7 # 750, column 8, lines 5-30) and provides means for resetting the SERDES (column 9, lines 45-60). It would have been obvious to one of ordinary skill in the art at the time the invention was made to enable Horowitz's apparatus to detect the output signals for misalignment and subsequently reset the SERDES upon detection of misalignment because one of ordinary skill in the art would have recognized that detecting misalignment or mismatches in the output signals is an essential part of transmitting signals and the encoding and transmission of signals will be useless unless the signals are transferred without errors. Further, resetting the SERDES to restart the encoding and transmission will prevent the apparatus from operating inefficiently.

As per claim 2:

Horowitz/Susnow teaches the system as rejected in claim 1 above, wherein the logic maintains a count of the number of mismatches, such system providing a reset

signal to the serializer-deserializer when a predetermined plurality of mismatches has been indicated (column 9, lines 45-6).

As per claim 3:

Horowitz/Susnow teaches a system analyzer, comprising; a transmitter board for transmitting a copy of signals being produced in a system for analysis by the system analyzer, the copy of such signals comprising serial data, each such data being in a series a low byte serial link and a high byte serial link, such signals including with the data and special characters interspersed in a pattern with the data in the low byte serial link and interspersed with the data in such high byte serial link (Figure 1B, see above); an analyzer board adapted for plugging into the transmitter board (Figure 1B, see above), such analyzer board comprising: a serializer-deserializer for receiving the transmitted serial data when the analyzer board is plugged into the transmitter board (Figure 1B, see above), and for converting the received data and the special characters interspersed therewith in the low byte serial link into corresponding a low byte parallel link and concurrently converting the received data and the special characters interspersed therewith in the low byte serial link into a corresponding high byte parallel link (Figure 1B, see above); a system for determining whether the data and interspersed pattern of special characters in the converted low byte parallel link mismatch the data and the interspersed pattern of special characters in the converted high byte parallel link (see above), a determined mismatch indicating the high byte parallel link is not aligned with the low byte parallel link, such system maintaining a count of the number of mismatches (see above), such system providing a reset signal to the serializer-

deserializer when a predetermined plurality of mismatches has been indicated (see above).

As per claim 4:

Horowitz/Susnow teaches a system analyzer, comprising; a transmitter board for transmitting a copy of signals being produced in a system for analysis by the system analyzer, the copy of such signals comprising serial data, each such data in the series having lower significant bytes thereof in a low byte serial link and having more significant bytes thereof in a high byte serial link, such signals including with the data, special characters interspersed in a pattern with the bytes of each of the data in such low byte serial link and interspersed with the bytes of each of the data in such high byte link serial data (Figure 1B, see above); an analyzer board adapted for plugging into the transmitter board (Figure 1B, see above), such analyzer board comprising: a serializer-deserializer for receiving the transmitted serial data when the analyzer board is plugged into the transmitter board (Figure 1B, see above), and for converting the received low significant bytes of each data and the special characters interspersed therewith in the low byte serial link into corresponding lower significant bytes in a parallel low byte link and concurrently converting the received higher significant bytes in each data and the special characters interspersed therewith in the low byte serial link into corresponding parallel higher significant bytes in a parallel high byte link (Figure 1B, see above); a system for determining whether the data and pattern of special characters in the parallel low byte link matches the data and the pattern of special characters in the parallel high byte link (see above), a determined match

indicating the high byte parallel link is aligned with the low byte parallel link and a mismatch indicating the high byte parallel link is not aligned with the low byte parallel link, such system maintaining a count of the number of mismatches (see above), such system providing a reset signal when a predetermined plurality of mismatches has been indicated (see above), and wherein the reset signal is fed to the serializer-deserializer to reset such serializer-deserializer (see above).

***Allowable Subject Matter***

The following is an Examiner's statement of indication of allowable subject matter:

The present invention includes an interface, comprising: a plurality of director boards; a plurality of memory boards, each one of the director boards being connected to the plurality of memory boards with a corresponding one of a plurality of point-to-point serial bus primary channels, a director board-to-memory board portion of each one of such primary channels passing signals from such one of the director boards and the corresponding one of the memory boards and a memory board-to-director board portion of each one of such primary channels passing signals from such corresponding one of the memory boards to such one of the director boards; primary channels passing signals from the one of the director boards connected thereto and receiving a copy of signals from the a memory board-to-director board portion of each one of such primary channels passing signals from the corresponding one of the director boards connected thereto, the copy of the memory board-to-director board portion having a high byte serial link and a low byte serial link and the copy of the memory board-to-director board

portion having a high byte serial link and a low byte serial link; a plurality of analyzer boards, each one being pluggable into a corresponding one of the adapter boards, each one of such analyzer boards, comprising: a serializer-deserializer for converting: the copy of the memory board-to-director board portion having the low byte serial link into a low byte parallel link representing the low byte serial link of the copy of the memory board-to-director board portion; the copy of the memory board-to-director board portion having the high byte serial link into a high byte parallel link representing the high byte serial link of the copy of the memory board-to-director board portion; the copy of the director board-to-memory board portion having the low byte serial link into a low byte parallel link representing the low byte serial link of the copy of the director board-to-memory board portion; and the copy of the memory board-to-director board portion having the high byte serial link into a high byte parallel link representing the high byte serial link of the copy of the director board-to-memory board portion; a logic for determining: whether the low byte parallel link representing the copy of the memory board-to-director board portion is aligned with the high byte, parallel link representing the copy of the memory board-to-director board portion; and whether the low byte parallel word representing the copy of the director board-to-memory board portion is misaligned with the high byte parallel link representing the copy of the director board-to-memory board portion; such logic producing a reset signal if such logic determines either: the low byte parallel link representing the copy of the memory board-to-director board portion is misaligned with the high byte parallel link representing the copy of the memory board-to-director board portion; or the low byte parallel link representing the

copy of the director board-to-memory board portion is misaligned with the high byte parallel link representing the copy of the director board-to-memory board portion; and wherein such reset signal is fed to the serializer-deserializer to reset such serializer-deserializer.

The prior arts of record Mayweather et al. US PG Pub no. 20020147947 A1, Horowitz et al. US Pat no. 7,142,612 B2 and Susnow et al. US Pat no. 6,747,997 B1 do not teach the same detailed structure of an interface circuit as claimed in claim 5. Hence, the prior arts of record fail to anticipate or render obvious the claimed system. Thus claims 5-9 are allowable over the prior arts of record.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Saqib Siddiqui
Art Unit 2138
05/22/2007

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PRIMARY EXAMINER